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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,772	08/01/2005	Christopher Rodd Speirs	CH02 0021 US	4888

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EXAMINER	
ABDIN, SHAHEDA A	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
09/19/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/518,772	SPEIRS ET AL.	
	Examiner	Art Unit	
	SHAHEDA A. ABDIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/25/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment field on 08/25/2008 has been entered and considered by Examiner.

2. Applicant's arguments, with respect to claim 14 have been fully considered. The claim rejection under 35 U.S.C. 112, first paragraph of claim 14 has been withdrawn. However, upon further consideration claim 14 has been rejected under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US. Patent No: 6323849 B1) in view of Duwaer et al. (US Patent No: 4922240).

(1) Regarding claim 9:

A row driver circuit (140) for controlling n rows (141-149) of a display device (150) that is operable in a partial mode (column 1, lines 53-61), the row driver circuit (140) having n outputs (i.e. outputs to the rows141-149), with a logic function (i.e. 110

having logic zero), wherein the logic function deactivates/activates the row outputs in dependence on the partial mode responsive to a first control signal.

Note that He teaches the logic function (i.e. 110 having logic zero) but He does not teaches the logic function connected in front of each of the row outputs.

However, Duwaer et al. in the same field of endeavor teaches logic function (I.e. 61-63 having h logic) is connected in the row drive circuit (row scanner) in front of each of row outputs (i.e. g_0-g_e) (see Fig. 2, Fig. 9,column 4, lines 43-44, and column 8, lines 41-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a method of logic function as taught by Duwaer in to the row driver of the display system of He so that a logic function could be connected in front of each of the row outputs wherein the logic function deactivates/activates the row outputs in dependence on the partial mode responsive to a first control signal. In this configuration system would have improve driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 67-68, column 4, lines 1-10).

(2) Regarding claim1:

He teaches a circuit arrangement for controlling a display device (150) which can be operated in a partial mode (column 1, lines 53-61) ,the circuit arrangement comprising a row drive circuit (140) for driving n rows (141-149) of the display device (150) and a column drive circuit (130) for driving m (131-139) columns of the display

device, wherein the row drive circuit (140) controls the n rows (141-149) of the display device sequentially from 1 to n (141-149), and the column drive circuit (130) supplies column voltages to the m columns (131-139), which the column voltages correspond to the picture data to be displayed of pixels of the controlled row, characterized in that a logic function (I.e. having logic zero) a first control signal (i.e. microprocessor 190 sends control signal pulse on a line control 105 via control circuit 130 via reset line 113 and reset low logic signal '0') is supplied, said first control signal (113) achieving a deactivation/activation (a fraction of display that can be turn off by the controller 110 which is connected to the row driver 140 turn, see column 3, lines 3-7) of the at least one row output (out put to the row lines 141-149) in dependence on the partial mode (partial display mode activating area) (column 2, lines 41-46, column 3, lines 1-30, fig. 1 and 2).

Note that He does not teach logic function is included in the row drive circuit in front of at least one row.

However, Duwaer et al. in the same field of endeavor teaches logic function (I.e. h logic) is included in the row drive circuit (row scanner) in front of each of at least one row (i.e. g_0-g_e) (see Fig. 2, Fig. 9,column 4, lines 43-44, and column 8, lines 41-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate a method of logic function as taught by Duwaer in to row driver of the display system of He so that the logic function could be included in the row drive circuit in front of at least one row output to which logic function a first control

signal being supplied the first control signal achieving a deactivation/activation of the at least one row output in dependence on the partial mode. In this configuration the system would have compact size and improve driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 67-68, column 4, lines 1-10).

(3) Regarding claim 2:

Duwaer discloses that the logic function is connected in front of each row output (see Fig. 2, Fig. 9,column 4, lines 43-44, and column 8, lines 41-55).

(4) Regarding claim 3:

Duwaer teaches that the logic function (i.e. 61-63 being) being realized as an AND Gate (see Fig. 9).

(5) Regarding claim 5:

He teaches that the first control signal (113) is capable of switching (reset from 'on' state to 'off' state) off all n row outputs (cleared of data) by means of the logic functions (220, 2300) during the control (control by the control circuit 110) of a line that is not to be displayed in the partial mode (note that When the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 (control by 110) based on the number of lines that have already been activated and the partial display control signals (i.e, screen has partial data) When the reset line 113 goes low, the shift registers of the column drivers 130, shown in FIG. 1 are cleared of data. By resetting the row and column drivers before the full display has been activated (column 3, lines 12-30).

(6) Regarding claim 6:

He teaches that a control logic (i.e. signal 113) in the column drive circuit (130) generates the first control signal in dependence on the partial mode and supplies the first control signal to the row driver circuit (140) (column 2, lines 41-46, column 3, lines 1-30, fig. 1).

(7) Regarding claim 7:

He teaches that the column drive circuit (130) supplies no column voltages to the m columns outputs (output to the data line 131 -139) in a case of a line that is not to be displayed (when the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 based on the number of lines that have already been activated and the partial display control signals; note that display portion or lines are controlled by a driving column voltage when the display portion is showing by lines in the display and driving in a manner that if there is no column voltage in certain lines, no display is available in that lines because pixel in a row occurred when voltage is applied to that pixel ; which means no column voltage is driving to the line in the case of a line that not to be displayed) (also see column (column 3, lines 12-30).

(8) Regarding claim 10:

He teaches that a display device (150) comprising a circuit arrangement (column 2, lines 41-46, column 3, lines 1-30 and Fig. 1 - 2).

(9) Regarding claim 11:

He teaches an electronic appliance (circuit) display device (150) (column 2, lines 41-46, fig 2-4).

(10) Regarding claim 12:

Note the discussion of He above in claim 1 which is similar to claim 12.Only the different, claim 1 is an apparatus and claim 12 is a method claim.

5. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over He in view of Duwaer as applied to claim 1 and further in view of Sarrasin et al. (US Patent No: 5600343).

(1) Regarding claim 4:

Note the discussion of He above. He teaches that the row driver circuit (140) comprise a shift register (column 3 lines 43-45) , but He does not disclose that the shift register has n stages and n outputs, and in that a second control signal can be supplied to the shift register at the input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal.

However, Sarrasin in the same field of endeavor discloses the shift register (30) has n stages (32_1-32_i) and n outputs (output at (34_1-34) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) thereof for controlling the consecutive rows (L1-Li), which second control signal activates the outputs (output at (34_1-34) of the shift register (30) consecutively in dependence on a clock signal (Cp) (column 5, lines 43-67, fig. 3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the shift register (30) which has n stages (32_1-32_i)

and n outputs (output at (34_1-34) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) as taught by Sarrasin in to the display system of He as modified by Duwaer so that for controlling the consecutive rows, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal . In this configuration the system would be provided a significant reduction of the electrical consumption as a function of the image to be displayed (Sararsin, column 3, lines 61-63).

(13) Regarding claim 13:

Sarasin teaches wherein each of the stages includes a flipflop (i.e. 32i) (column 6, lines 43-53, and fig. 3).

(14) Regarding claim 14:

Duwaer discloses the first control signal (i.e. V_{Blank}) overrides the second control signal (e.g. 68 in the shift register) (see Fig. 9, column 13, lines 17-30) (note that the second control signal i.e. 68 is applied to the output lines 70 subsequently to the selective row output lines if the first control signal i.e. V_{Blank} is terminated. Thus, the first control signal (V_{Blank}) override the second control signal 68).

(2) Regarding claim 8:

Sarrasin teaches that the frequency of the clock signal (Cp) can be increased in the case of one or several consecutive rows (unused rows) that is or are not to be

displayed (note that for each rising of the clock Cp the position of logic level '1' is on D then a logic '0' for all following clock stork. It should be noted that '0' is corresponds to the unselected rows, therefore, frequency of the signal will be increased in a manner -+ -+ that frequency of the clock Cp can be increased when the respective row line is turning off for the deactivator partial turning off position (see column 6, lines 17-35).

Response to Arguments

6. Applicant's arguments, with respect to claim 1-12 have been considered but are not persuasive.

(A) Applicant argues that (1) He's reference does not teach a display circuit arrangement that include a row driver circuit having a logic function connected in front of the row outputs. (2) "Duwaer does not teach a partial mode scheme (i.e. where an unneeded portion of the display is deactivated to save power)", (3) Applicant further argues that " nothing in Duwaer to teach or suggest the claimed feature of supplying a control signal to the logic function to activate and deactivate row outputs based on a partial mode address scheme. Therefore, proposed combination does not teach or suggest the claimed invention.

In response 1, 2 and 3, Examiner respectfully disagree applicant's point of view. Note that the rejection is based on the reference of He in view of Duwaer. He's reference explicitly teaches the claim limitations including the logic function (i.e. 110

having logic zero) as discussed in the rejection of claim 9 above, but He does not teaches the logic function connected in front of each of the row outputs. However, Duwaer teaches logic function (I.e. 61-63 having h logic) is connected in the row drive circuit (row scanner) in front of each of row outputs (i.e. g_0-g_σ) (see Fig. 2, Fig. 9,column 4, lines 43-44, and column 8, lines 41-55).

In response 2 and 3, Examiner disagree Applicant's point of view. It should be noted that the limitation "partial mode" for achieving deactivation/activation is broadly recited in the claim and Duwaer's reference teaches this limitation. The reference of Duwaer teaches a matrix display in such that the switching signals comprises an ON state to activate a row conductor and on Off state when the row conductor is deactivated (column 15, lines 63-68). More over in column 7, lines 60-68, Duwaer discloses that at time T1 the first 40 video signals appear on lines V, C0(1) and Ce (1) are turned ON, C0(2) .... C0(16) and Ce(2).... C0(16) remain off. Alternately, at time T2, the next 40 video signals appear on lines V, Co(2) and Ce(2) are turned ON (the remaining control lines remain off), and the next set of signals are passed on to the matrix. At the end of 26 .mu.S, one line of the matrix can be activated. In column 8, lines 45-55, Duwaer discloses that the odd row lines are activated in odd rows frame and even row lines are activated I even row frame. Moreover, frame of the odd rows can be first activated followed by a frame of the even row. After all the even row lines become activated while the odd lines become inactive. Base on this, disclosure it is clearly shows that Duwaer's reference teaches the partial mode. Thus, combining the

reference of He and Duwaer would have been obvious to a person of ordinary skill in the art. In doing so the system would have improve driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 67-68, column 4, lines 1-10). In the obviousness teaching is that the method of Duwaer could be incorporated to the system of He. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

(B) Applicant specifically argues that " one of ordinary skill in the art would also not seek to modify He by replacing the control circuit with logic circuitry connected in front of the row outputs because the control circuit of He is meant to control both the row drivers and the column drivers".

In response, Examiner disagree Applicant's point of view. Note that He's reference is enough to teach the claim invention. However, Examiner introduced the Duwaer's reference only to teach the logic function which is connected in the row drive circuit (row scanner) in front of each of row outputs. Thus, combining the reference of He and Duwaer would have been obvious to a person of ordinary skill in the art. In doing so the system would have improve driving circuit for accurate data transmission in the display device (Duwaer, column 3, lines 30-50, lines 67-68). In the obviousness

teaching is that the method of Duwaer could be incorporated to the row driver of He. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

7. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to **Shaheda Abdin** whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard HJerpe** could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pari-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shaheda Abdin

09/12/2008

/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629